APPENDIX - (BLACK-LINE COPY) SHOWING CHANGES TO CLAIMS

Please amend Claims 1-7, 9-13, 15, and 17-18, as follows. Below are black-line copies of the amended claims showing the changes to the claims.

1. (Amended) A process for fabricating an integrated circuit, comprising:

[the production of] producing several metallization levels, which are mutually separated by interlevel insulating layers; [layers, and of]

producing intertrack insulating layers each separating [the] tracks of the same metallization level; and [, and the production of]

producing at least one capacitor comprising a lower electrode and an upper electrode which are mutually separated by a dielectric layer, wherein the production of the at least one capacitor comprises:

[the simultaneous production] simultaneously producing, in at least part of an intertrack insulating layer associated with a [given] particular metallization level, on the one hand, [of the two electrodes] the lower electrode, the upper electrode, and [of] the dielectric layer of the at least one capacitor and, on the other hand, [of] simultaneously producing a conducting trench which laterally extends the lower electrode of the capacitor, is electrically isolated from the upper electrode and has a transverse dimension smaller than the transverse dimension of the capacitor; and

[the production] producing, in the interlevel insulating layer covering the intertrack insulating layer, [of] two conducting pads which come into contact with the upper electrode of the capacitor and with the conducting trench, respectively.

2. (Amended) The process according to Claim 1, wherein the trench comprises only the conducting material forming the [first] lower electrode.

3. (Amended) The process according to Claim 1, wherein the tracks of [the given] a particular metallization level are produced simultaneously with the formation of the upper electrode of the capacitor.

4. (Amended) The process according to Claim 1, wherein the production of the capacitor and of the trench comprises:

a) [the] formation of the intertrack insulating layer on an interlevel insulating layer;

b) [the] etching [of] at least part of the intertrack insulating layer so as to form a cavity having a main part laterally extended by the trench;

c) [the] formation of a first conducting layer of a first conducting material on the structure obtained in step b) and [the] formation of a dielectric layer of a dielectric material on the first conducting layer;

d) [the] formation of a second conducting layer of a second conducting material on the dielectric layer so as to fill the main part of the cavity, the dimensions of the trench and the [thicknesses] thickness of the first conducting layer and of the dielectric layer being chosen so as to obtain, after step d), a trench comprising at least the first conducting material but not containing the second conducting material; and

e) chemical-mechanical polishing of the multilayer stack formed in steps c) and d) so as to leave, in the main part of the cavity, the capacitor whose lower electrode is formed from a residual part of the first layer coating [the] of internal walls of the cavity and whose upper electrode is formed from a residual part of the second layer, which is separated from the residual part of the first layer by a residual part of the dielectric layer, and to leave, in the trench, another residual part of the first layer coating of at least [the] internal walls of the trench, to the exclusion of any residual part of the second layer.

5. (Amended) The process according to Claim 4, wherein the trench comprises only the conducting material forming the [first] lower electrode.

6. (Amended) The process according to Claim 4, wherein the tracks of [the given] a particular metallization level are produced simultaneously with the formation of the upper electrode of the capacitor.

7. (Amended) The process according to Claim 4, wherein the production of the tracks of [the given] a particular metallization level comprises:

after step c), etching [of] the dielectric layer [,] of the first conducting layer and of the intertrack insulating layer so as to form at least one auxiliary trench;

the [deposition] formation of the second conducting layer being carried out in step d) so as to substantially fill the trench [or trenches]; and

the chemical-mechanical polishing being carried out in step e) so as to remove the first conducting layer, the dielectric layer and the second conducting layer from the surface of the intertrack insulating layer.

9. (Amended) The process according to Claim 8, wherein the trench comprises only the conducting material forming the [first] lower electrode.

10. (Amended) The process according to Claim 8, wherein the tracks of [the given] a particular metallization level are produced simultaneously with the formation of the upper electrode of the capacitor.

11. (Amended) The process according to Claim 10, wherein the production of the tracks of [the given] a particular metallization level comprises:

after step c), etching of the dielectric layer, of the first conducting layer and of the intertrack insulating layer so as to form at least one auxiliary trench;

the deposition of the second conducting layer carried out in step d) so as to fill the trench or trenches; and

the chemical-mechanical polishing carried out in step e) so as to remove the first conducting layer, the dielectric layer and the second conducting layer from the surface of the intertrack insulating layer.

12. (Amended) An integrated circuit comprising several metallization levels, which are mutually separated by interlevel insulating layers, and intertrack insulating layers each separating the tracks of the same metallization level, and at least one capacitor comprising a lower electrode and an upper electrode which are mutually separated by a dielectric layer, wherein the capacitor is located in at least part of an intertrack insulating layer associated with a [given] particular metallization level, in that the lower electrode of the capacitor is laterally extended by a conducting trench, which is electrically isolated from the upper electrode and has a transverse dimension smaller than the transverse dimension of the capacitor, and in that the integrated circuit comprises, in the interlevel insulating layer covering the intertrack insulating layer, two conducting pads which come into contact with the upper electrode of the capacitor and with the conducting trench, respectively.

13. (Amended) The integrated circuit according to Claim 12, wherein the tracks of [the given] a particular metallization level are formed from the material as that forming the upper electrode of the capacitor.

15. (Amended) The integrated circuit according to Claim 14, wherein the tracks of [the given] a particular metallization level are formed from the material as that forming the upper electrode of the capacitor.

17. (Amended) The integrated circuit according to Claim 16, wherein the tracks of [the given] a particular metallization level are formed from the material as that forming the upper electrode of the capacitor.

18. (Amended) An integrated circuit comprising:

a plurality of metallization levels that are mutually separated by interlevel insulating layers, and intertrack insulating layers each separating the tracks of the same metallization level; and

at least one capacitor comprising a lower electrode and an upper electrode, which are mutually separated by a dielectric layer, and wherein the capacitor is located in at least part of an intertrack insulating layer associated with a [given] particular metallization level, in that the lower electrode of the capacitor is laterally extended by a conducting trench, which is electrically isolated from the upper electrode and has a transverse dimension smaller than the transverse dimension of the capacitor, and wherein, in the interlevel insulating layer covering the intertrack insulating layer, two conducting pads come into contact with the upper electrode of the capacitor and with the conducting trench, respectively, and wherein the tracks of the [given] particular metallization level are formed from the material as that forming the upper electrode of the capacitor.

REMARKS

Reexamination and reconsideration of this application as amended is requested. By this amendment Claims 1-7, 9-13, 15, and 17-18, have been amended. After this amendment, Claims 1-18 remain in the application.

Claim Rejections – 35 USC § 112, Second Paragraph

(1 - 4) The Examiner rejected Claims 1, 3, 4, 6-8, 10-13, 15, and 17-18, under 35 U.S.C. § 112, second paragraph, for failing to particularly point out and distinctly claim the subject matter of the invention. The Examiner specifically pointed out certain claim language that would require clarification.

Applicants have amended Claims 1, 3, 4, 6-7, 10-13, 15, and 17-18, to more clearly and distinctly recite the present invention, in accordance with Examiner's suggestions. The purpose of the amendment is to correct minor formality and not to limit in any way the present claims for patentability. No new matter has been added.

Specifically, with respect to Examiner's inquiry regarding the meaning of the language "simultaneous production ..." in Claim 1, Applicants first of all direct particular attention to the specification, on page 4, lines 19-23, where it is stated that "the invention, by simultaneously producing the capacitor and the lateral trench, provides for the contacting of the two electrodes of the capacitor from the top of the integrated circuit. The invention therefore in no way requires the formation, prior to that of the capacitor, of a lower contact pad for connection to the lower electrode." Additionally, please note, as illustrated in FIGs. 1, 2, 3a, and 3b, and that:

- By a same etching step, the cavity 4 is produced, comprising the main part 40 and the lateral trench 41. Thus, the main part 40 and the lateral trench 41 are produced simultaneously;

- After this etching step, layers 5, 6 and 7 are formed on the substrate covering the filling both main part 40 and lateral trench 41 of the cavity;
- After that, a chemical-mechanical polishing is made, so as to obtain the structures illustrated in figures 3b and 4b. Consequently, the isolated trench 41 and the capacitor have been formed simultaneously, i.e. by using a same etching step, a same deposition of layers, and a same polishing step.

Accordingly, Applicants believe that the "simultaneously production" language, as used in Claim 1, should be more clearly understood.

Specifically, with respect to Examiner's inquiry regarding the location of "auxillary trench" in Claim 7, and with respect to the difference between the "auxillary trench and the conducting trench in Claim 1, as discussed for the exemplary embodiment in the specification, please note that the conducting trench is in contact with the lower electrode of the capacitor and allows a contact of the lower electrode from the top of the integrated circuit. The auxiliary trench, which is also obtained simultaneously with the upper electrode of the capacitor, is a metal track of the metallization level M2 (see, for example, page 11, lines 6 and following).

Specifically, with respect to Examiner's inquiry regarding the meaning of "less than twice the sum of the thickness of the first conducting layer and of the thickness of the dielectric layer" in Claim 8, please see FIGs. 2 and 4a, and the discussion in the specification, for example, on page 5, lines 17-21, and page 9, lines 26-28, and page 10, line 32, to page 11, line 4.

Specifically, with respect to Examiner's inquiry regarding the meaning of simultaneously forming the metallization (90) and the upper electrode (70) as shown in FIGs. 10-11, with reference to Claims 3, 6, and 10, the Examiner's understanding is

correct. See page 11, lines 24-26.

Specifically, with respect to Examiner's inquiry regarding the term "the given metallization", with reference to Claims 3, 6, 13, 15, 17, and 18, Applicants have amended the Claims 3, 6, 13, 15, 17, and 18, to more clearly refer to "a particular metallization". Please also note, for example, that the auxiliary trench, which is also obtained simultaneously with the upper electrode of the capacitor, is a metal track of the metallization level M2 (see page 11, lines 6 and following).

Specifically, with respect to Examiner's inquiry regarding the term "the first electrode", with reference to Claim 2, Applicants have amended the term to more clearly identify the "lower electrode".

Specifically, with respect to Examiner's inquiry regarding the term "the etching", and the term "internal walls" with reference to Claim 4, Applicants amended Claim 4 to more clearly recite the etching step and also to refer to the internal walls of the cavity and the trench. Please also refer to the specification, on page 5, lines 9-15, and see FIGs. 1 and 2, illustrating a cavity 4 and a trench 41.

Accordingly, Applicants believe that, in view of the discussion above, the Claims 1, 3, 4, 6-8, 10-13, 15, and 17-18, now recite clearly and distinctly, and that the rejection of the Claims 1, 3, 4, 6-8, 10-13, 15, and 17-18, under 35 U.S.C. § 112, second paragraph, has been overcome by the amendment and remarks above.

Claim Rejections – 35 USC § 102(e)

(5 - 7) The Examiner rejected Claims 1-4 and 6-9 under 35 U.S.C. § 102(e) as being anticipated by Brabazon et al., U.S. Patent No. 6,008,083. Additionally, the Examiner rejected Claims 1-18 under 35 U.S.C. § 102(e) as being anticipated by Bernstein et al., U.S. Patent No. 6,452,251.

First of all, with respect to the Brabazon reference, please note that the Brabazon patent has been cited by Applicants in the present specification (page 3, lines 5-10). And, as mentioned, the production of the capacitor in the Brabazon document requires, prior to the production of the lower electrode, the formation of a pad contacting this lower electrode and produced within the lower metallization level.

By contrast, the presently claimed invention in no way requires the formation, prior to that of the capacitor, of a lower contact pad for connection to the lower electrode." (See for example the specification, on page 4, lines 21-23). The presently claimed "simultaneously producing...", as recited for independent Claim 1, and for all dependent claims depending therefrom, including dependent Claims 2-4 and 6-9, is clearly not taught, anticipated, or suggested, by the cited Brabazon reference.

Turning now to the Bernstein reference, the Examiner particularly focuses on Figure 1K. The Examiner considers that the capacitor would be constituted by the lower electrode 41, the dielectric layer 49, and the top electrode 51. Further, the Examiner considers that a trench, formed by layers 41 and 43, would extend laterally from the lower electrode. The Examiner considers also that a pad 75 contacts the top electrode, whereas the lower electrode would be connected through the trench 41-43 by a pad 77.

However, Applicants respectfully disagree with, and traverse, the Examiner's analysis of the Bernstein patent. As a matter of fact, the lower electrode of the capacitor is connected to metallization 23 by a via 39. Please note that the via 37 and, consequently, the pad 77, cannot be connected to the lower electrode since layer 71 is an insulating layer. See also Bernstein reference, at column 5, lines 33-34. Therefore, Applicants believe that the Bernstein reference does not teach, anticipate, or suggest, the presently claimed invention, as recited for independent Claims 1, 12, and 18, and for all dependent claims depending therefrom, respectively.

Accordingly, since the presently claimed limitations, as discussed above, are not taught, anticipated, or suggested by the Brabazon cited reference, nor by the Bernstein cited reference, Applicants believe that the rejection of Claims 1-4 and 6-9 under 35 U.S.C. § 102(e) as being anticipated by Brabazon, and the rejection of Claims 1-18 under 35 U.S.C. § 102(e) as being anticipated by Bernstein, both have been overcome by the amendment and remarks above, and Applicants urge the Examiner to allow these claims in their present form.

The foregoing is submitted as full and complete response to the Official Action mailed September 25, 2002, and it is submitted that Claims 1-18 are in condition for allowance. Reconsideration of the rejections is requested. Allowance of Claims 1-18 is earnestly solicited.

The present application, after entry of this amendment, comprises eighteen (18) claims, including three (3) independent claims. Applicants have previously paid for twenty (20) claims including three (3) independent claims. Applicants, therefore, believe that an additional fee for claims is currently not due.

However, a petition for a two (2) month extension of time to file this Response has been attached to this Response with amendment. The Commissioner is hereby authorized to charge the extension fee in the amount of $410 to Deposit Account No. 50-1556.

If the Examiner believes that there are any informalities which can be corrected by Examiner's amendment, a telephone call to the undersigned at (561) 989-9811 is respectfully solicited.

The Commissioner is hereby authorized to charge any fees which may be required or credit any overpayment to Deposit Account 50-1556.

In view of the preceding discussion, it is submitted that the claims are in condition for allowance.

Respectfully submitted.

Dated: February 25, 2003 By: Jose Gutman

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